CIRCUIT FOR GENERATING A DATA STROBE SIGNAL USED IN A DOUBLE DATA RATE SYNCHRONOUS SEMICONDUCTOR DEVICE

ABSTRACT

Provided is a circuit for generating a data strobe signal used in a double data rate (DDR) synchronous semiconductor device. The circuit comprises a first logic unit capable of generating a pull up control signal responsive to first and second clock signals. A second logic unit is capable of generating a pull down signal responsive to the first and second clock signals. A data strobe buffer is capable of generating a data strobe signal responsive to the pull up and pull down control signals, the data strobe signal including a preamble. The first logic unit is capable of generating the preamble responsive to a first pulse of the first clock signal. And the data strobe signal is in a high impedance state responsive to a last pulse of the first clock signal.